[0013] Multi-component low-k isolation spacers may be used to isolate any conductive region in a semiconductor structure. FIG. **1** illustrates a cross-sectional view representing a conductive region isolated by a pair of two-component low-k isolation spacers, in accordance with an embodiment of the present invention. A conductive region **102** sits above a structure **104** (e.g. a portion of a plurality of interconnects, a semiconductor substrate or an array of semiconductor or electronic devices) and is flanked by a pair of two-component isolation spacers **106**, comprised of upper portions **106**A and lower portions **106**B. In one embodiment of the present invention, both upper portion **106**A and lower portion **106**B are directly adjacent to the same sidewall of conductive region **102**, as depicted in FIG. **1**. The widths of upper portion **106**A and lower portion **106**B need not be the same, however, upper portion **106**A should be sufficiently wide as to protect the more fragile lower portion **106**B during processing steps. In one embodiment, the width of upper portion **106**A is the same as the width of lower portion **106**B, as depicted in FIG. **1**. In another embodiment, the width of upper portion **106**A is greater than the width of lower portion **106**B by at least 10 Angstroms. In an embodiment, the width of the top surface of lower portion **106**B is in the range of 30-250 Angstroms and the width of bottom surface of upper portion **106**B is in the range of 40-400 Angstroms. Lower portion **106**B should be of a height sufficient to significantly reduce the fringe capacitance between conductive region **102** and another conductive region. In one embodiment, lower portion has a height of at least 50 Angstroms. Meanwhile, upper portion **106**A should be of a height sufficient to protect lower portion **106**A during processing steps. In an embodiment, upper portion has a height of at least 200 Angstroms.

[0014] Two-component isolation spacer **106**, comprised of upper portion **106**A and lower portion **106**B, may be formed from any dielectric materials capable of suppressing a current flow. The dielectric constant of upper portion **106**A should be different from the dielectric constant of lower portion **106**B, otherwise a single-component isolation spacer would likely be sufficient. In fact, the dielectric constant of the more robust upper portion **106**A should be greater that that of lower portion **106**B. Otherwise, in accordance with an embodiment of the present invention, lower portion **106**B would not provide the desired reduction in fringe capacitance. Thus, in accordance with an embodiment of the present invention, the dielectric constant of upper portion **106**A is greater than the dielectric constant of lower portion **106**B. In one embodiment, the dielectric constant of lower portion **106**B is in the range of 2.0-4.0 and the dielectric constant of upper portion **106**A is in the range of 4.0-7.5. In another embodiment, the dielectric constant of upper portion **106**A is at least twice the dielectric constant of lower portion **106**B. In an embodiment, lower portion **106**B is comprised of silicon dioxide and upper portion **106**A is comprised of a material selected from the group consisting of silicon nitride, silicon oxy-nitride and carbon-doped silicon nitride. In one embodiment, the dielectric constant of lower portion **106**B is in the range of 2.5-3.5. In an embodiment, lower portion **106**B is comprised of a material selected from the group consisting of a porous film or a fluorinated oxide.

[0015] Conductive region **102** may be any conductive region in a semiconductor structure. For example, in accordance with an embodiment of the present invention, conductive region **102** is a gate electrode in a MOS-FET device. Thus, in one embodiment, structure **104** is a semiconductor substrate comprising a channel region. In an embodiment, conductive region **102** is a gate electrode comprised of doped polycrystalline silicon or a silicide thereof. In another embodiment, conductive region **102** is a gate electrode comprised of a metal layer such as but not limited to metal nitrides, metal carbides, hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel or conductive metal oxides, e.g. ruthenium oxide. When conductive region **102** is a gate electrode, it may further comprise a gate dielectric layer between the gate electrode and structure **104**. In one embodiment, the gate dielectric layer is formed by a thermal oxidation process and is comprised of silicon dioxide or silicon oxy-nitride. In another embodiment, the gate dielectric layer is formed by chemical vapor deposition or atomic layer deposition and is comprised of a high-k dielectric layer such as, but not limited to, hafnium oxide, zirconium oxide, hafnium silicate, hafnium oxy-nitride or lanthanum oxide.

[0016] In accordance with an alternative embodiment of the present invention, conductive region **102** is an interconnect from a plurality of interconnects that connect various electronic and semiconductor devices into a global circuitry. Thus, structure **104** may comprise a portion of a plurality of interconnects or an array of semiconductor or electronic devices. In one embodiment, structure **104** is a layer of metal interconnects. In another embodiment, structure **104** is an array of complimentary metal-oxide-semiconductor (CMOS) transistors incased in a dielectric layer. The interconnect **102** may comprise any suitable material that can conduct a current. In one embodiment, the interconnect is comprised of copper, silver, aluminum or an alloy thereof. In another embodiment, the interconnect comprises an array of interspersed carbon nanotubes. The interconnect may comprise a barrier layer, which may comprise any material suitable to inhibit electro-migration within a plurality of interconnects, to prevent oxidation of the interconnect or to provide a surface for nucleation in a damascene process. In one embodiment, the barrier layer is comprised of tantalum, titanium, tantalum nitride, titanium nitride or a combination thereof. The interconnect may also comprise a capping layer. In an embodiment, the capping layer comprises iridium, ruthenium, cobalt, cobalt/tungsten alloy, cobalt/tungsten phosphide, cobalt boron phosphide or a combination thereof.

[0017] A replacement isolation spacer technique may be used to incorporate a multi-component low-k isolation spacer into a semiconductor structure with a conductive region, e.g. a gate electrode. FIGS. **2**A-K illustrate cross-sectional views representing the formation of a planar MOS-FET with a gate electrode isolated by a pair of two-component low-k isolation spacers, in accordance with an embodiment of the present invention.

[0018] Referring to FIG. **2**A, a gate electrode **202** may be formed above a substrate **204**. Substrate **204** may be non-insulating and may comprise a semiconducting material or epitaxial layer. In one embodiment, substrate **204** is formed by doping a crystalline silicon, germanium or silicon/germanium layer with an appropriate charge carrier, such as but not limited to phosphorus, arsenic, boron, indium or a combination thereof. In another embodiment, substrate **204** is comprised of a III-V material such as but not limited to gallium nitride, gallium phosphide, gallium arsenide, indium phosphide or indium antimonide. In one embodiment, substrate **204** is comprised of an epitaxial layer grown atop a